Listing of Claims:

1. (Currently amended) A method for displaying timing data generated by simulating a circuit being designed by an EDA tool ~~design~~, the method comprising:

receiving the timing data from ~~an~~ the EDA tool;

selecting first and second signals applied to nodes internal to the circuit based on input received from a user;

generating a first waveform for the first signal and a second waveform for the second signal using the timing data;

displaying a portion of each of the first and second waveforms in an interactive graphical user interface, wherein the portion of each of the first and second waveform displayed in the interface includes time points of interest to the user;

displaying pointers to the time points of interest on the first and second waveforms;

receiving edits to the time points of interest in response to a user moving the pointers on the interactive graphical user interface; and

updating timing parameters based on the edits to the time points of interest to simulate the circuit.

2. (Previously presented) The method of claim 1 further comprising:

transmitting the updated timing parameters back to the EDA tool;

generating updated first and second waveforms for the first and second signals using updated timing data received from the EDA tool, wherein the updated timing data is generated by simulating the circuit design using the updated timing parameters; and

displaying the updated first and second waveforms in the interactive graphical user interface.

3. (Previously presented) The method of claim 1 wherein:

displaying the portion of each of the first and second waveforms in the interactive graphical user interface further comprises displaying a first waveform of a first clock signal received at a first storage element, and a second waveform of a second clock signal received at a second storage element.

4. (Previously presented) The method of claim 3 wherein:

displaying the portion of each of the first and second waveforms in the interactive graphical user interface further comprises displaying a third waveform of the first clock signal at first clock source, and a fourth waveform of the second clock signal at a second clock source,

the first waveform of the first clock signal being delayed with respect to the third waveform by a first clock skew value, and the second waveform of the second clock signal being delayed with respect to the fourth waveform by a second clock skew value.

5. (Previously presented) The method of claim 3 wherein

displaying the portion of each of the first and second waveforms in the interactive graphical user interface comprises displaying a launch edge of the first clock signal at which the first storage element releases a data signal, and displaying a latch edge of the second clock signal at which the second storage element captures the data signal.

6. (Previously presented) The method of claim 5 wherein:

the interactive graphical user interface displays portions of the first waveform of the first clock signal and the second waveforms of the second clock signal that each start with a point in time corresponding to a period before both the launch and latch edges and end with a point in time corresponding to a period following both of those edges.

7. (Original) The method of claim 5 wherein:

the launch edge is a first time point of interest identified by a first one of the pointers on the interactive graphical user interface; and

the latch edge corresponds to a second time point of interest identified by a second one of the pointers on the graphical user interface.

8. (Original) The method of claim 5 wherein:

updating the timing parameters based on the edits to the time points of interest further comprises updating a multi-cycle value that represents a number of active edges in the second clock signal between the launch edge and the latch edge.

9. (Original) The method of claim 5 wherein:

updating the timing parameters based on the edits to the time points of interest further comprises inverting the launch edge of the first clock signal, either in a design file or as an input to a static timing verification tool.

10. (Original) The method of claim 5 wherein:

updating the timing parameters based on the edits to the time points of interest further comprises inverting the latch edge of the second clock signal.

11. (Currently amended) A computer-readable medium encoded with a computer program, the computer program comprising a set of instructions for providing timing data generated by simulating a circuit ~~design~~ being designed using an EDA tool, wherein the set of instructions when executed by a computer cause the computer to:

enable selection of signals applied to nodes internal to the circuit based on an input received from a user;

generate at least first and second waveforms for signals using the timing data;

display a portion of each of the at least first and second waveforms in an interactive graphical user interface, wherein the portion of each of the at least first and second waveforms displayed in the interactive graphical user interface includes time points of interest to the user;

display pointers to the time points of interest on the waveforms;

generate new timing parameters based on edits to the time points of interest received from the user, wherein the user moves the pointers on the interactive graphical user interface to generate the edits;

generate updated waveforms for the signals using updated timing data, wherein the EDA tool generates the updated timing data by compiling, simulating and performing verification analysis on the circuit design using the new timing parameters; and

display the updated waveforms in the interactive graphical user interface.

12. (Previously presented) The computer-readable medium according to claim 11 wherein:

the display of the portion of each of the waveforms in the interactive graphical user interface further comprises display of each of the portions of the waveforms in synchronism.

13. (Previously presented) The computer-readable medium according to claim 11 wherein:

the timing data generated by the EDA tool includes periods of a plurality of clock signals, duty cycles of the clock signals, offsets between the clock signals, and clock skews between sources of the clock signals and circuit elements that receive the clock signals.

14. (Previously presented) The computer-readable medium according to claim 11 wherein:

the display of the portion of each of the waveforms in the interactive graphical user interface further comprises display of a first waveform of a first clock signal received at a first circuit, and display of a second waveform of a second clock signal received at a second circuit.

15. (Previously presented) The computer-readable medium according to claim 14 wherein:

the display of the portion of each of the waveforms in the interactive graphical user interface further comprises display of a third waveform of the first clock signal at a first clock source, and a fourth waveform of the second clock signal at a second clock source,

wherein the first waveform is delayed with respect to the third waveform by a first clock skew value, and the second waveform is delayed with respect to the fourth waveform by a second clock skew value.

16. (Previously presented) The computer-readable medium according to claim 15 wherein the display of the pointers to the time points of interest on the waveforms further comprises:

display of a first pointer to a launch edge of the first waveform that triggers a first latch to capture a data signal; and

display of a second pointer to a latch edge of the second waveform that triggers a second latch to capture the data signal.

17. (Previously presented) The computer-readable medium according to claim 16 wherein the display of the pointers to the time points of interest on the waveforms further comprises:

display of a third pointer to an edge of the third waveform that corresponds to the launch edge of the first waveform; and

display of a fourth pointer to an edge of the fourth waveform that corresponds to the latch edge of the second waveform.

18. (Previously presented) The computer-readable medium according to claim 16 wherein the computer generates:

the new timing parameters based on the edits to the time points of interest by changing a multi-cycle value that represents a number of active edges in the second clock signal from the launch edge to the latch edge in response to the user moving the first or the second pointer on the interactive graphical user interface.

19. (Previously presented) The computer-readable medium according to claim 17 wherein the computer generates:

the new timing parameters based on the edits to the time points of interest by changing a multi-cycle value that represents a number of active edges in the second clock signal from the launch edge to the latch edge in response to the user moving the third or the fourth pointer on the interactive graphical user interface.

20. (Previously presented) The computer-readable medium according to claim 11 wherein the circuit design is a design for a field programmable gate array.